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TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. ITL.0644US

In Re Application Of: **Christopher J. Kelly et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
09/955,230	09/18/01	Tuan T. Dinh	2827

Invention: **Printed Circuit Board Routing And Power Delivery For High Frequency Integrated Circuits**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **March 12, 2004**

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Signature

Dated: **March 17, 2004**

Fred G. Pruner, Jr., Reg. No. 40,779
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Suite 100
Houston, Texas 77024
(713) 468-8880
(713) 468-8883 (fax)

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Janice Munoz

Signature of Person Mailing Correspondence

Janice Munoz

Typed or Printed Name of Person Mailing Correspondence

cc:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicants:	Christopher J. Kelly, et al.	§	Art Unit:	2827
Serial No.:	09/955,230	§	Examiner:	Tuan T. Dinh
Filed:	September 18, 2001	§		
Title:	Printed Circuit Board Routing and Power Delivery for High Frequency Integrated Circuits	§	Docket No.	ITL.0644US (P12307)

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPEAL BRIEF

Dear Sir:

Applicant hereby appeals from the Final Rejection dated January 16, 2004, finally rejecting claims 1-29.

I. REAL PARTY IN INTEREST

The real party in interest is Intel Corporation, the assignee of the present application by virtue of the assignment recorded at Reel/Frame 012181/0632.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

Date of Deposit. March 17, 2004
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Janice Munoz

III. STATUS OF THE CLAIMS

Claims 1-29 have been finally rejected and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

There are no unentered amendments.

V. SUMMARY OF THE INVENTION

Referring to Fig. 2, an embodiment 30 of a printed circuit board (PCB) 30 in accordance with the invention is constructed to minimize the degree of noise that the PCB 30 induces on high frequency signals that propagate across the PCB 30. In particular, the PCB 30 includes a top signal layer 34 that includes embedded supply voltage planes 46 (one embedded supply voltage plane 46 being depicted in Fig. 2) and an adjacent supply voltage plane layer 36 that is located below the layer 34 and includes embedded ground planes 70 (one embedded ground plane 70 being depicted in Fig. 2). As described below, each high frequency component that is mounted on the top side of the PCB 30 is located near and is coupled to one embedded supply voltage plane 46 and one embedded ground plane 70 for purposes of minimizing inductances that may otherwise be introduced by the PCB 30. Although a four layer PCB is described, the arrangements described herein are not limited to four layer PCBs and thus, may be applied to other multiple layer PCBs, such as six and eight layer PCBs, for example. Specification, p. 3.

Thus, due to this arrangement, the current return paths for signals propagating in

the top signal layer 34 do not pass through the relatively thick (as compared to the conductive layers) substrate, or core 37 of the PCB 30. Therefore, parasitic inductances otherwise induced by the PCB 30 are minimized. Furthermore, as described below, due to this arrangement, a low-noise, high quality and highly-decoupled path between a supply voltage and a particular die pad may be created. Specification, p. 3.

More particularly, in general, the top signal layer 34 includes a signal region 44 that includes traces to communicate various non-supply voltage related signals. The supply voltage planes 46 are surrounded by this region 44, and each supply voltage plane 46 is associated with and located near supply voltage pins 52 of a particular associated high frequency component (such as the component 50) for purposes of providing a supply voltage to the component 50. As described below, in some embodiments of the invention, each supply voltage plane 46 has an outer boundary that is generally established by the supply voltage pins 52 of the associated component 50 so that the pins 52 vertically extend into the associated plane 56 near the plane's outer periphery. Specification, p. 3.

For each high frequency component that is mounted to the top side of the PCB 30, the supply voltage plane layer 36 includes an associated embedded ground plane 70. In this manner, the supply voltage plane layer 36 generally includes a region 72 to communicate a supply voltage to components of the PCB 30. The ground plane(s) 70 of the PCB 30 are surrounded by this region 72. In some embodiments of the invention, each ground plane 70 has a boundary that is generally defined by the locations of ground vias 39 that extend from the signal trace region 44 of the top layer 34 to the ground plane

70 for purposes of establishing a return current path for an electrical device (resistor or capacitor, for example) that is connected to the high frequency component 50. For example, an electrical device 53 may be connected between an electrical trace 45 that extends to a pin 54 of the component 50 and the via 39. The ground plane 70 is generally larger in size than the associated supply voltage plane 46, is located directly beneath and separated by only one of the insulating layers 20 from the associated supply voltage plane 46. In some embodiments of the invention, the ground plane 70 circumscribes the projection of the supply voltage plane 46 onto the supply voltage plane layer 36. Specification, pp. 3-4.

In some embodiments of the invention, each supply voltage plane 46 is coupled to the region 72 of the supply voltage plane layer 36 by way of an inductive element 80 (a ferrite bead inductor, for example) that has one terminal that is coupled to the embedded supply voltage plane 46. The other terminal of the inductive element 80 is coupled to a signal trace 49 (in the signal communication region 44 of the signal layer 34) that couples the inductive element 80 to a via 73. The via 73 vertically extends to connect the region 46 (of the supply voltage layer 36) to the inductive element 80 and thus, couple the region 72 to the supply voltage plane 46. Specification, p. 4.

Each ground plane 70 is coupled to a ground plane layer 38 (of the PCB 30) by way of a via 45 that vertically extends between the ground plane 70 and the ground plane layer 38. The ground plane layer 38 is located next to the substrate 39 on the opposite side of the substrate 39 from the layers 34 and 36. Specification, p. 4.

Among other possible layers of the PCB 30, the PCB 30 may include at least one

additional signal layer, such as a signal layer 40 that may form the bottom layer of the PCB 30, for example. Specification, p. 4.

As a more specific example of the relationship of a particular high frequency component 50 to the associated embedded supply voltage plane 46 and embedded ground plane 70, Fig. 3 depicts a schematic top view of the PCB 30 near the high frequency component 50. In other embodiments of the invention, the component 50 may have a different shape (a square shape, as an example) and may have supply voltage pins that are not necessarily located near its four corners. Furthermore, the component 50, in some embodiments of the invention, may have a package, such as ball grid package (for example), that does not use the die pads that are depicted in Fig. 3. Specification, pp. 4-5.

As shown in Fig. 3, for this example, the component 50 includes supply voltage pins 52 that are located near the four corners of the generally rectangular (from the top view) component 50. The supply voltage pins 52 extend vertically into the embedded supply voltage plane 46, and as shown, the associated embedded supply voltage plane 46 extends beneath the main body of the component 50 and extends inside the signal pins 57 of the component 50. The outer periphery of the supply voltage plane 46 extends closely around the ground pins 54 of the component 50 and extends from underneath the main body of the component 50 to allow the supply voltage pins 52 to extend downwardly to contact the supply voltage plane 46. Specification, p. 5.

The ground plane 70 extends a sufficient distance about the component 50 so that the ground vias 39 may extend downwardly to make electrical connections with the

ground plane 70. As depicted in Fig. 3, a signal trace 81 extends from an inductive element 80 to the via 73 extends beyond the embedded ground plane 70 and into the region 72 of the supply voltage plane layer 36. Specification, p. 5.

Fig. 4 depicts a more specific example of the signal layer 34 in accordance with an embodiment of the invention. The signal layer region 44 (i.e., the region in Fig. 4 other than the supply voltage plane 46) includes pads 98 for mechanically and electrically connecting the pins of the component 50 to the PCB 30 using solder connections between the pins and the pads 98. The pads 98 in this example are generally arranged in two parallel rows, and the embedded supply voltage region 46 extends between these two parallel rows of pads 98. Other arrangements/organizations are possible for the pads 98, in other embodiments of the invention. Specification, p. 5.

As depicted in Fig. 4, the signal layer region 44 also includes signal traces 45a that are used to communicate signals between the component 50 and other components mounted to the PCB 30. The signal layer region 44 also includes signal traces 45b that are connected to the vias 39 (not shown in Fig. 4) that extend to the embedded ground region 70 of the layer 36 as well as possibly extend to the ground layer 38. Specification, pp. 5-6.

Fig. 5 depicts a more specific example of the supply voltage plane layer 36 in accordance with an embodiment of the invention. Also depicted in Fig. 5 is a projection 100 of the component 50 on the layer 36. As shown, the ground plane 70 surrounds a region around the projection 100 to allow vias to extend from all high frequency signal traces associated with the component 50 to the embedded ground plane 70. Part of the

region 72 (of the layer 36), which surrounds the embedded ground plane 70, is also depicted in Fig. 5. Specification, p. 6.

Referring to Figs. 6 and 7, the layers of the PCB 30 have been discussed in association with a particular high frequency component 50. However, the PCB 30 may have more than one high frequency component, and thus, the PCB 30 may have multiple embedded supply voltage planes 46 within a top signal layer 34a. Corresponding to the signal layer 34a, the supply voltage plane layer 36 includes embedded ground planes 70, each of which is associated with and larger than a corresponding one of the embedded supply voltage planes 46. Specification, p. 6.

Although the various embodiments have been described herein using orientational terms, such as "top," "bottom," etc., such orientations are used for purposes of simplifying discussion of these embodiments and are not necessary to practice the invention. Specification, p. 6.

VI. ISSUES

A. Can claims 1-14 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 1?

B. Can claims 15-19 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 15?

C. Can claims 20-26 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 20?

D. Can claims 27-29 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 27?

VII. GROUPING OF THE CLAIMS

Claims 1-14 can be grouped together; claims 15-19 can be grouped together; claims 20-26 can be grouped together; and claims 27-29 can be grouped together. With this grouping, all claims of a particular group stand or fall together. Furthermore, regardless of the grouping set forth by the Examiner's rejections, the claims of each group set forth in the section stand alone with respect to the other groups. In other words, any claim of a particular group set forth in this section, does not stand or fall together with any claim of any other group set forth in this section.

VIII. ARGUMENT

All claims should be allowed over the cited references for the reasons set forth below.

A. Can claims 1-14 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 1?

The printed circuit board of independent claim 1 includes a printed circuit board substrate, a signal layer and a supply plane. The signal layer is supported by the printed circuit board substrate and includes traces to communicate signals that are not associated with regulated supply voltages. The supply voltage plane is supported by the printed circuit board substrate and is embedded in the signal layer to supply power to multiple supply voltages pins of a component that is mounted to the printed circuit board.

The Examiner rejects independent claim 1 under 35 U.S.C. § 103(a) over U.S. Patent No. 6,064,113 (herein called "Kirkman") in view of U.S. Patent No. 6,307,769 (herein called "Nuxoll"). Kirkman generally describes a semiconductor device package, a cross-section of which is depicted in Figure 3. More specifically, Figure 3 of Kirkman depicts a first signal layer 80, a ground plane 82, a combined ground and power plane 84 and a second signal layer 86. Figure 3 of Kirkman also discloses traces 46 and 48 that appear to be part of the first signal layer 80. Kirkman discloses that the traces 46 and 48 are rings that are connected by vias to ground and power planes. *See, for example*, Kirkman, 7:33-40.

Nuxoll generally describes a memory module that includes a module board 31 that is depicted in Figure 3A, for example, of Nuxoll.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 1 for at least the reason that even assuming, *arguendo*, that the combination of Kirkman and Nuxoll is proper, the combination fails to teach or suggest all claim

limitations. More specifically, the Examiner relies on Kirkman to allegedly teach the supply voltage plane of independent claim 1. Claim 1 recites that the supply voltage plane is embedded in a signal layer; and the Examiner refers to the traces 46 and 48 as allegedly teaching a power plane that is embedded in the first signal layer 80 (depicted in Figure 3 of Kirkman). However, Kirkman clearly describes the traces 46 and 48 as rings that are connected by vias *to the ground and power planes. (emphasis added). See, for example,* Kirkman, 7:33-40. Thus, Kirkman fails to use the terminology "planes" in the description of the traces 46 and 48 and makes a distinction between its ground and power planes and the traces 46 and 48. Therefore, when a reasonable construction is assigned to the terms to independent claim 1, it becomes apparent that Kirkman fails to teach or suggest a supply voltage plane that is embedded in a signal layer, as the traces 46 and 48 are not supply voltage planes. Instead, Kirkman describes a ground plane 82 and a combined ground and power plane 84; and as is clearly illustrated in Figure 3, these planes 82 and 84 are neither embedded in the first signal layer 80 nor the second signal layer 86. Thus, Kirkman fails to teach or suggest the supply voltage plane of independent claim 1.

Likewise, Nuxoll simply teaches a memory module and fails to teach or suggest the supply plane of independent claim 1.

Therefore, for at least the reason that the combination of references fails to teach or suggest all limitations of independent claim 1, a *prima facie* case of obviousness has not been established for this claim.

A *prima facie* case of obviousness has not been established for independent claim 1 for at least the additional, independent reason that the Examiner fails to show where the prior art contains the alleged suggestion or motivation to combine Kirkman and Nuxoll to derive the claimed invention. The Examiner, having knowledge of the claimed invention, combines Nuxoll and Kirkman in a piecemeal fashion to derive the claimed invention. However, a mere conclusion of obviousness is not sufficient to establish a *prima facie* case of obviousness. Rather, the Examiner must show that one skilled in the art, *without knowledge of the claimed invention*, would have combined Nuxoll and Kirkman to derive the claimed invention. The Examiner has failed to make this showing, as the Examiner merely concludes a case of obviousness without showing any reasoning or cited prior art language to support this conclusion.

As further evidence of a lack of a suggestion or motivation to combine Nuxoll and Kirkman to derive the claimed invention, Kirkman clearly teaches away from the claimed invention and from its combination with Nuxoll. For example, in lines 15-23 in column 3 of Kirkman, Kirkman teaches that different techniques are desired to reduce the overall size of the semiconductor device package. Therefore, this is further evidence that one skilled in the art would not have been motivated to use Kirkman in the design of a memory module that includes a printed circuit board substrate, as Kirkman teaches the miniaturization of a semiconductor device package in stark contrast to motivating one skilled in the art to take Kirkman's teachings and apply it to a printed circuit board. References cannot be combined when one of the references teaches away from their

combination; and references cannot be combined when one of the references teaches away from the claimed invention. M.P.E.P. § 2145

Therefore, for at least the additional, independent reason that the Examiner has failed to show where the prior art contains the alleged suggestion or motivation to combine Nuxoll and Kirkman to derive the claimed invention, a *prima facie* case of obviousness has not been established for independent claim 1.

Claims 2-14 are patentable for at least the reason that these claims depend from an allowable claim. Therefore, the § 103(a) rejections of claims 1-14 are in error and should be reversed.

B. Can claims 15-19 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 15?

The printed circuit board of independent claim 15 includes a printed circuit board substrate, a supply voltage plane layer and a ground plane. The supply voltage plane layer is supported by the printed circuit board substrate and communications a supply voltage. The ground plane is supported by the printed circuit board substrate and is embedded in the supply voltage plane layer to provide ground connections to multiple pins of a component that is mounted to the printed circuit board.

The Examiner rejects independent claim 15 under 35 U.S.C. § 103(a) over Kirkman in view of Nuxoll.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 15 for at least the reason that the Examiner fails to show where the prior art

contains the alleged suggestion or motivation for the combination of Kirkman and Nuxoll. A *prima facie* case of obviousness requires more than just a piecewise combination of elements from various references. Rather, a *prima facie* case of obviousness requires a suggestion or motivation in the prior art for the combination of references, as "obviousness cannot be predicated on what is unknown." *In re Spormann*, 363 F.2d 444, 448, 150 USPQ 449, 452 (CCPA 1966); M.P.E.P. § 2143. Additionally, the Examiner must support the allegation of the suggestion or motivation in the prior art with a specific citation to a prior art reference showing where the prior art reference contains the alleged suggestion or motivation. *Ex parte Gambogi*, 62 USPQ2d 1209, 1212 (Bd. Pat. App. & Int. 2001); *In re Rijckaert*, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); M.P.E.P. § 2143.

Thus, for at least the reason that the Examiner fails to show where the prior art contains the alleged suggestion or motivation for the combination of Kirkman and Nuxoll to derive the claimed invention, a *prima facie* case of obviousness has not been established for independent claim 15. As pointed out above in the discussion of Issue A, Kirkman, in fact, teaches away from the claimed invention and from its combination with Nuxoll, thereby further providing evidence that no suggestion or motivation in the art exists for the combination of Nuxoll and Kirkman to derive the claimed invention.

Claims 16-19 are patentable for at least the reason that these claims depend from an allowable claim. Thus, the § 103 rejections of claims 15-19 are in error and should be reversed.

C. Can claims 20-26 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 20?

The method of independent claim 20 includes for each high frequency component to be mounted on a printed circuit board, embedding an associated supply voltage plane in a signal layer of the printed circuit board to provide power to the component. Claim 20 recites that the signal layer is used to communicate high frequency signals that are associated with the high frequency component or components.

The Examiner rejects independent claim 20 under 35 U.S.C. § 103(a) in view of the combination of Kirkman and Nuxoll.

The Examiner fails to establish a *prima facie* case of obviousness for independent 20 for at least the reason that even assuming, *arguendo*, that the combination of Nuxoll and Kirkman is proper, this combination fails to teach or suggest all claim limitations. For example, the Examiner fails to show where either reference teaches embedding a supply voltage plane in a signal layer of a printed circuit board. The Examiner refers to the traces 46 and 48, depicted in the first signal layer 80 of Kirkman, as allegedly teaching a supply voltage plane embedded in a signal layer. However, Kirkman clearly distinguishes the traces 46 and 48 from its disclosed power plane, i.e., the combined ground and power plane 84. In fact, Kirkman simply describes the traces 46 and 48 as vias to connect ground and power planes. *See, for example*, Kirkman, 7:33-40. Thus, the Examiner is assigning an unreasonable construction to "supply voltage plane," thereby improperly ignoring limitations of independent claim 20. Nuxoll fails to teach or suggest the missing claim limitations.

Therefore, for at least the reason that the combination of Nuxoll and Kirkman fails to teach or suggest all claim limitations, a *prima facie* case of obviousness has not been established for independent claim 20.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 20 for at least the additional, independent reason that the Examiner fails to show where the prior art contains the alleged suggestion or motivation for the combination of Nuxoll and Kirkman. Furthermore, Kirkman teaches away from its combination with Nuxoll and teaches away from the claimed invention, as discussed above in connection with Issue A. Thus, for at least this additional, independent reason that the Examiner fails to show where the prior art contains the alleged or motivation for the combination of Kirkman and Nuxoll to derive the claimed invention, a *prima facie* case of obviousness has not been established for independent claim 20.

Claims 21-26 are patentable for at least the reason that these claims depend from an allowable claim. Therefore, the § 103 rejections of claim 20-26 are in error and should be reversed.

D. Can claims 27-29 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 27?

The method of independent claim 27 includes for each high frequency component to be mounted on a printed circuit board, embedding an associated ground plane in a supply voltage plane of the printed circuit board to provide ground connections for the

component. The supply voltage plane is used to communicate a supply voltage to the high frequency component or components.

The Examiner rejects independent claim 27 under 35 U.S.C. § 103(a) over Kirkman in view of Nuxoll. However, the Examiner fails to show where the prior art contains the alleged suggestion or motivation to combine Nuxoll, a reference directed to a memory module that has a printed circuit board with Kirkman, a reference directed to a semiconductor device package. Furthermore, Kirkman discloses a goal of miniaturizing its semiconductor device package, contrary to the combination of Kirkman with Nuxoll, a reference that describes a memory module on a printed circuit board. Thus, the Examiner has failed to show why one skilled in the art, *without knowledge of the claimed invention*, would have combined Nuxoll and Kirkman to derive the claimed invention; and Kirkman, in fact, teaches away from this combination thereby providing evidence that such a suggestion or motivation does not exist in the prior art.

Claims 28 and 29 are patentable for at least the reason that these claims depend from an allowable claim. Thus, the § 103(a) rejections of claims 27-29 are in error and should be reversed.

IX. CONCLUSION

Applicant requests that each of the final rejections be reversed and that the claims subject to this appeal be allowed to issue.

Respectfully submitted,

Date: March 17, 2004

Fred G. Pruner, Jr., Reg. No. 40,779
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Suite 100
Houston, TX 77024-1805
713/468-8880 [Phone]
713/468-8883 [Facsimile]

APPENDIX OF CLAIMS

The claims on appeal are:

1. A printed circuit board comprising:

a printed circuit board substrate;

a signal layer supported by the printed circuit board substrate, the signal layer comprising traces to communicate signals not associated with regulated supply voltages; and

a supply voltage plane supported by the printed circuit board substrate, the supply voltage plane embedded in the signal layer to supply power to multiple supply voltage pins of a component mounted to the printed circuit board.

2. The printed circuit of claim 1, further comprising:

a supply voltage plane layer separate from the signal layer.

3. The printed circuit board of claim 1, wherein the supply voltage plane has an outer boundary established by the supply voltage pins of the component.

4. The printed circuit board of claim 1, wherein the supply voltage plane lies substantially within a region located directly below the component, the component being mounted on top of the signal layer.

5. The printed circuit board of claim 1, wherein the supply voltage plane has an outer boundary that generally follows a projection of a main body of the component onto the signal layer.

6. The printed circuit board of claim 1, further comprising:

a supply voltage plane layer different from the signal layer, the supply voltage plane layer comprising an embedded ground plane to provide ground connections for the signal layer.

7. The printed circuit board of claim 6, wherein the ground connections are associated with electrical devices connected to the component.

8. The printed circuit board of claim 6, wherein the ground plane has an outer boundary established by the ground connections.

9. The printed circuit board of claim 6, wherein the ground plane lies substantially within a region located directly below the component, the component being mounted on top of the signal layer.

10. The printed circuit board of claim 6, wherein the ground plane is significantly larger than the supply voltage plane.

11. The printed circuit board of claim 6, wherein the ground plane has an outer boundary that circumscribes a projection of the supply voltage plane onto the supply voltage plane layer.

12. The printed circuit board of claim 6, further comprising:

a core layer,

wherein the signal layer and the supply voltage plane layer are located on the same side of the core layer.

13. The printed circuit board of claim 6, wherein the ground plane reduces an inductance.

14. The printed circuit board of claim 1, wherein the supply voltage reduces an inductance.

15. A printed circuit board comprising:

a printed circuit board substrate;

a supply voltage plane layer supported by the printed circuit board substrate, the supply voltage plane layer to communicate a supply voltage; and

a ground plane supported by the printed circuit board substrate, the ground plane embedded in the supply voltage plane layer to provide ground connections to multiple pins of a component mounted to the printed circuit board.

16. The printed circuit of claim 15, further comprising:

a ground plane layer separate from the supply voltage plane layer.

17. The printed circuit board of claim 15, wherein the ground plane lies substantially within a region located directly below the component, the component being mounted on top of a signal layer.

18. The printed circuit board of claim 15, wherein the ground connections are associated with electrical devices connected to the component.

19. The printed circuit board of claim 15, wherein the ground plane has an outer boundary established by the ground connections.

20. A method comprising:

for each high frequency component to be mounted on a printed circuit board, embedding an associated supply voltage plane in a signal layer of the printed circuit board to provide power to the component, the signal layer being used to communicate high frequency signals associated with the high frequency component or components.

21. The method of claim 20, further comprising:

coupling the supply voltage plane or planes embedded in the signal layer to a supply voltage plane layer separate from the signal layer.

22. The method of claim 21, wherein the coupling comprises:

coupling an inductive element between at least one of the supply voltage plane or planes embedded in the signal layer and the supply voltage plane layer.

23. The method of claim 20, further comprising:

locating each supply voltage plane embedded in the signal layer underneath the associated component, the component or components being mounted on top of the signal layer.

24. The method of claim 20, further comprising:

for each supply voltage plane embedded in the signal layer, embedding an associated ground plane in a supply voltage plane layer of the printed circuit board to provide ground connections for the component associated with said supply voltage plane embedded in the signal layer.

25. The method of claim 24, further comprising:

providing a core to support the signal layer and the supply voltage plane layer; and

locating the signal layer and the supply voltage plane layer on the same side of the core.

26. The method of claim 25, further comprising:

providing a ground plane layer on the opposite side of the core from said same side of the core; and

connecting the ground plane or planes embedded in the supply voltage plane layer to the ground plane layer.

27. A method comprising:

for each high frequency component to be mounted on a printed circuit board, embedding an associated ground plane in a supply voltage plane layer of the printed circuit board to provide ground connections for the component, the supply voltage plane layer being used to communicate a supply voltage to the high frequency component or components.

28. The method of claim 27, further comprising:

coupling the ground plane or planes embedded in the supply voltage plane layer to a ground plane layer separate from the supply voltage plane layer.

29. The method of claim 27, further comprising:

locating each ground plane embedded in the supply voltage plane layer underneath the associated component, the component or components being mounted above the supply voltage plane layer.